Akul Malhotra

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Education

Purdue University **Jan. 2021 – Present**
Ph.D. in Electrical and Computer Engineering *West Lafayette, Indiana, USA*

BITS Pilani **Aug. 2016 – Jul. 2020**
B.E. in Electrical and Electronics Engineering *Pilani, Rajasthan, India*

Professional Summary

I am pursuing my PhD in the field of **algorithm-hardware codesign** for resource-efficient and robust **deep learning (DL) accelerators**, with an emphasis on **Computing-in-Memory (CiM)** based memory design using CMOS and post-CMOS memories. I am seeking an **internship** in this field for **Summer 2024**.

Coursework & Technical Skills

Coursework (Hardware): Advanced VLSI Design, Digital VLSI Design, CMOS Analog IC Design, Digital Systems Design Automation, Computer Architecture, Solid State Devices
Coursework (Algorithms): Deep Learning (DL), Optimization for DL, Applied Algorithms, Linear Algebra
Languages: Python, C++, MATLAB, Verilog-A, C, Java, R, HTML
Software: HSPICE, Cadence Virtuoso, Cadence Layout XL, Ansys Totem, Synopsys Nanotime, Simulink, EagleCAD
Frameworks: Pytorch, Tensorflow, LaTeX

Experience

MediaTek Inc. **May. 2023 – Aug. 2023**
Custom SRAM Design Intern *Austin, Texas, USA*

- Worked on **timing closure** for various custom SRAM caches using **Synopsys Nanotime**.
- Proposed **Electromigration (EM)** and **IR-drop** fixes for multiple custom SRAM caches using **Ansys Totem**.
- Explored **low power/high performance SRAM** design for a **2D vector computing engine**.

Purdue University **Jan. 2021 – Present**
Research Assistant *Ph.D. Advisor: Dr. Sumeet K. Gupta*

- Developed a **fault detection** and **correction** scheme for Compute-in-Memory (CiM) enabled **ternary neural network** (TNN) accelerators, which provided inference accuracy improvement of up to **40.68%**.
  - Design Automation Conference (DAC) 2023
- Proposed a **weight mapping scheme** for CiM enabled **binary neural network** (BNN) accelerators that simultaneously provides **weight encryption** and improves stuck-at fault robustness by up to **10.55%**.
  - Asia Pacific Design Automation Conference (ASP-DAC) 2024
- Designed a **voltage biasing scheme** for one-shot Computation in-Memory (CiM) of **Boolean logic functions** in both SRAMs and non-CMOS memories, leading to a decrease in energy-delay product (EDP) of up to **72.6%**.
  - IEEE Transactions on Circuits and Systems (TCAS) II
- Utilized a **Sharpness-aware minimization** training algorithm to design cycle-to-cycle variation and fault tolerant **sparse** deep neural network accelerators, with up to **19.5% accuracy improvement**.

Neuromorphic Computing Lab **Aug. 2019 – Jan. 2020**
Research Assistant *Penn State University, Pennsylvania*

- Implemented a **Bayesian deep neural network** for image classification using magnetic tunnel junction (MTJ) memory based crossbar-arrays, enhancing the network's energy efficiency by upto **24× during inference**.
  - IEEE Transactions on Electron Devices
- Exploited the cycle-to-cycle variations of **resistive random-access memories (RRAMs)** to design a **true** Gaussian random number generator.
  - **IEEE Transactions on Nanotechnology**